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THE STUDY AND INVESTIGATION OF POTENTIAL FAILURE MODES, EFFECT AND CRITICALITY IN 4 KVA INVERTER SYSTEMS

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ABSTRACT*: This research presented the study of potential failures, investigation of reliabilities and the analysis of failure modes, effect and their criticalities associated with a modularized 4 KVA inverter systems. The intent of the inverters' systems as commonly used alternative source to the mains required it continuously uninterrupted. These requirements have become even more relevant in view of the high sensitivity and sophistication of modern technological equipment presently in use. With this recommendation, the inverters' reliability and failure modes become paramount to be investigated and studied. The research depicts that the more the components connected to a section or unit of an inverter system, the higher the tendency of failure in such section and vice-versa. Also, the disparity between availability and reliability was also investigated and it was found that availability is a function of time while reliability is a function of the circuit components and not of time. On the final note, we believe the results and findings discussed in this research would provide guide to the designer of inverter system engineers in making informed choices on the likely failure modes, their criticality, probability of occurrence, severity and the risk preference number associated with all the possible failure modes.*

KEYWORDS*: Criticality, Inverter System, Reliability, Failure modes, and FMECA*

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I. INTRODUCTION

The increase in demand for electricity and the epileptic nature of power supply in Nigeria has led to increased demand for alternative sources of electrical energy. The most common alternative sources of power supply widely deployed are the inverters and generator systems. The cost of fuelling and maintaining generators to power critical business processes makes business overhead inconveniently high and prohibitive for the survival, growth of new businesses which contribute to the reduction of Gross Domestic Product (GDP) and thereby producing a negative effect on the economy of Nigeria. Power electronic solutions such as inverters which convert direct current (obtainable from renewable energy sources: solar and wind) to alternating current for domestic, commercial and industrial use are gaining increasing attention due to their environmental friendliness and low maintenance cost.

According to the recommendation made by the Institute of Electrical Electronics Engineers (IEEE), the alternative supplies that should be available for use should be continuously uninterrupted with constant frequency within the load determined in terms of voltage and current. These requirements have become even

more relevant in view of the high sensitivity and sophistication of modern technological equipment in use today. With this recommendation, the inverters which make use of the indestructible and free source of solar energy are used to address these issues, provided its reliability and failure modes can be ascertained. The Failure Modes, Effects and Criticality Analysis (FMECA) are evaluation procedures designed to identify potential failure modes for system design, to identify the risk associated with these failure modes, to classify the failures according to their severity and to carry out corrective actions in addressing the most severe fault. Each potential failure mode is classified according to its impact (severity) on the functionality of the system, personnel or equipment safety. On this note, the FMECA tools were used to determine the potential failure modes that are associated with a 4 kVA inverter systems, the effect of the failure modes and its criticality on the workability of the 4kVA was the main aim of this research work and the objectives are stated:

a) To generate the fault tree algorithms in carrying out the fault tree analysis.
b) To provide a basis for identifying root failure causes and developing corrective actions.
c) To facilitate investigation of design alternatives to consider high reliability at the conceptual stage of the design.
d) To provide a basis for qualitative reliability, maintainability, safety and logistic analyses.
e) To determine the effects of each failure mode on system performance.

II. RELATED RESEARCH WORK

The quest to investigate the failure modes of various systems and equipment through failure mode effect and critical analysis (FMECA) is gaining more and more attention in recent time. This reliability tool was originally developed in the 1940s by the U.S military, which published MIL P1629. By the early 1960s, contractors for the United State National Aeronautics and Space Administration (NASA) were using variation of FMECA under a variety of names. In 1966 NASA released its FMECA procedure which was officially used for the Apollo program in the United State of America's aerospace industry.

In the early 70s, Ford Motor Company began using FMECA after the problems they experienced with their Pinto model, and by 1980s FMECA has gained broad use in the automotive industry.

In the early 1980s, FMECA entered the microelectronics industry, and the Federal Aviation Administration also expressly required aviation system design and analysis process must be carried out with FMECA.

In 1983, the Military-Standard of -1629A (MIL-STD-1629A) replaced both MIL-STD-1629 and the 1977 aeronautical FMECA standard MIL-STD-2070. MIL-STD-1629A was cancelled without replacement in 1988, but nonetheless remains in wide use for military and space application today.

In 1992 William K. Denson of IIT Research Institute carried out an assessment of critical electronic components. In their research, data were collected from military maintenance records, warranty records, published information and field operations to support the model development. After the intensive research work, a new failure rate model was developed to model the failure rate of devices that exhibit worn-out failure mechanism.

In 1998, Joint Electron Device Engineering Council published *"Potential Failure Mode and Effects Analysis"*the latest version is JEP 131A-2005. This publication applies to electronic components, subassemblies products, process development, manufacturing processes and the associated performance requirements in customer application. The purpose of this document is to establish a minimum guideline for the application of FMECA techniques to improve quality, reliability, and consistency of electronic components subassemblies by continually evaluating the product or process against potential failure modes.

In 2006, Department of the Army TM 5-698-4, issued by the United State Department of the Army, presented equipment FMECA process for command, control, communications, computer, intelligence, surveillance and reconnaissance facilities.

In 2012, Godfrey *et al*., presented the development and analysis of fault tree diagram for the production section/line of a soft drink bottling company in Benin City Nigeria. Finally the research shows that the resultant fault tree diagram validated the ten first – order set which was seen as a valid path of occurrence of the top event.

In another relation in 2015, Raja *et al*.,carried out a review of the lead acid battery performance related to the manufacturing process of lead acid batteries to reflect the significant and impact of batteries performance on their life span. The research agreed that the analysis allows the determining, classifying and analyzing

common failures in lead acid battery manufacturing. As a result, an appropriate risk scoring of occurrence, detection and severity of failure modes and computing the Risk Priority Number (RPN) for detecting high potential.

Also in 2017, Omar *et al.*, studied the implementation of a methodological guide for the maintenance of photovoltaic system in Senegal. After the analysis the results allow the detection of 40% of the types of failure that caused over 60% of system malfunction.

In 2018, an investigation on the application of Fault Tree Analysis (FTA) on CNC training center was presented by Rajkumar*et al*. In the research work, major faults associated with the system and their causes are presented graphically and Boolean algebra was used in evaluating the FTA diagram to facilitate the derivation of governing reliability model for CNC turning center.

Dobrivoje*et al*., in 2019 presented an FMECA research which relies on existing standard that can be applied with reservation when the intensity of all modes of failure of element of mechanical systems and their ranking by degree of criticality is known. This is important because it points to the element and their failure modes on which a criticality is the greatest.

In each of the reviewed literatures, potential failure is ranked by the severity of its effect so that, corrective actions may be taken to eliminate or control design risk. High risk items are those items whose failure would alter the system functionality or endanger personnel.

III. RESEARCH METHODOLOGY

The inverter system was modularized as presented by the block diagram of Fig. 1 into five different units or modular stages to facilitate the investigation of the failure modes and its effect on the inverter systems. The development of the FTA for each of the inverter stages, development of the fault tree diagram (FTD) for each of the inverter stages, calculation of the failure rate for each of the stages and the calculation of the system reliability for each of the circuit section and proffer an investigative analysis over the variation of time to study the effect of the failure rate and reliability on the inverter system.

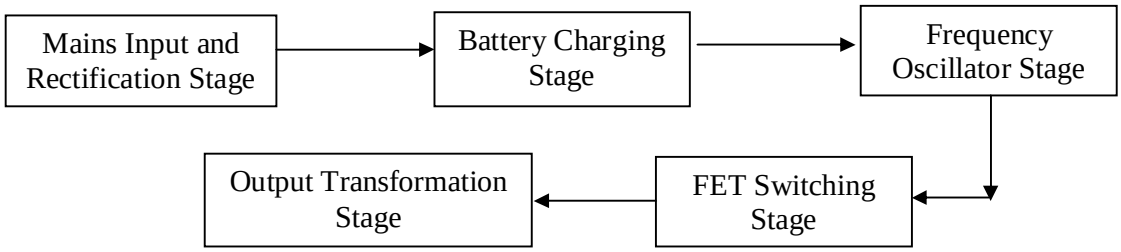

Fig. 1: The Basic and Simple Modularized Stages of the Inverter System.

A. THE FAULT TREE ALGORITHMS

These algorithms are developed using the fault tree techniques and syntax with the combination of the logic gates of AND and OR gates. In this research work, the inverter's circuit diagram was sub divided into five different units or modular stages for ease of analysis. Presented in Table 1 is the Fault Tree Algorithms (FTA) for each of the five stages.

Table 1: The Fault Tree Algorithms of the Inverter Systems Sub Stages

S/N	INVERTER UNIT	ALGORITHMS
1	Rectification Stage	The DC rectified output voltage will fail, if the step down transformer **OR** the diode in the bridge rectification fails. The diode in the bridge rectification will fail if there is diode primary failure. The transformer will fail if there is short circuit in the winding of the transformer (transformer primary failure) **OR** if there is primary power supply failure.

2	Charging Stage	The battery will fail to charge if there is battery primary failure **OR** if the NPN transistor Q1 is not biased **AND** the charging voltage is not up to the required voltage from the rectification circuit. The rectification circuit will fail if there is rectification circuit primary failure. The NPN transistor Q1 will fail if the LM324 comparator fail, the LM 324 will fail if the variable **AND** fixed resistor fails **OR** if the Zener diode fails primarily
3	Oscillator Stage	The oscillation of 50Hz generation will fail if the oscillation IC fail **OR** if voltage regulator 7805 IC primary failure. The oscillation IC will fail if there is oscillation IC primary failure **OR** if there is resistor **AND** capacitor primary failure.
4	Switching Stage	The switching of the gangs MOSFET will fail if there is MOSFET primary failure **OR** if the NPN transistor fail **AND** there is resistance primary failure. The NPN transistor will fail if there is primary failure of the two 1K resistance connected in parallel.
5	Output Transformation Stage	The output voltage will fail if there is output transformation failure. The transformer will fail if there is winding primary failure **OR** if there is switching section primary failure.

B. THE FAULT TREE DIAGRAM (FTD)

The Fault Tree Analysis (FTA), is a top-down deductive failure analysis in which an undesired state of a system is analyzed using Boolean logic to combine a series of lower-level events. Mostly, the fault tree diagrams are developed from the fault tree algorithms. In this regard, the five modularized stages of the 4 kVA inverter systems whose algorithms are presented in Table 1 are therefore developed and presented in Fig. 2 to Fig. 6.

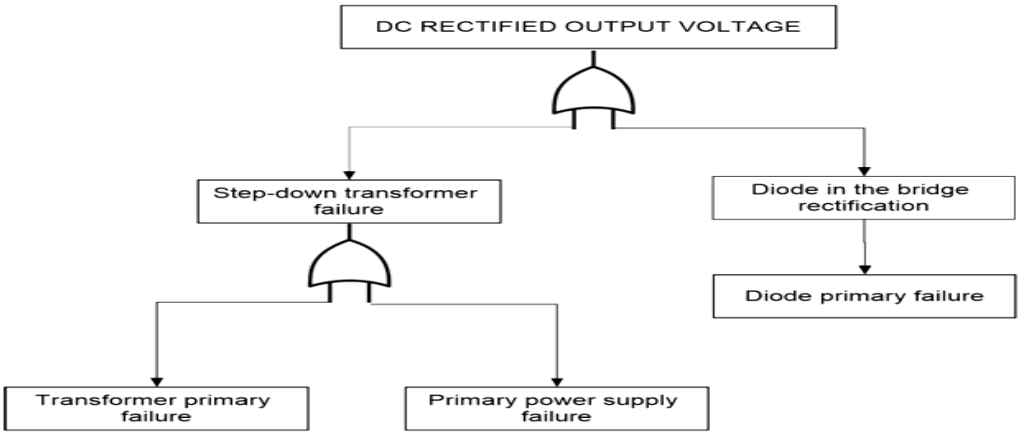

Fig. 2: FTD of the DC Rectified Output Unit

The Fault Tree Diagram of the DC rectified output voltage was made the top event as shown in Fig.2.The failure rate of the top event was estimated from the primary failures of other components that are present in the rectification circuit. The FTD diagram of Fig. 2 consists of two OR logic gates as explained in the fault tree algorithms presented in Table 1.

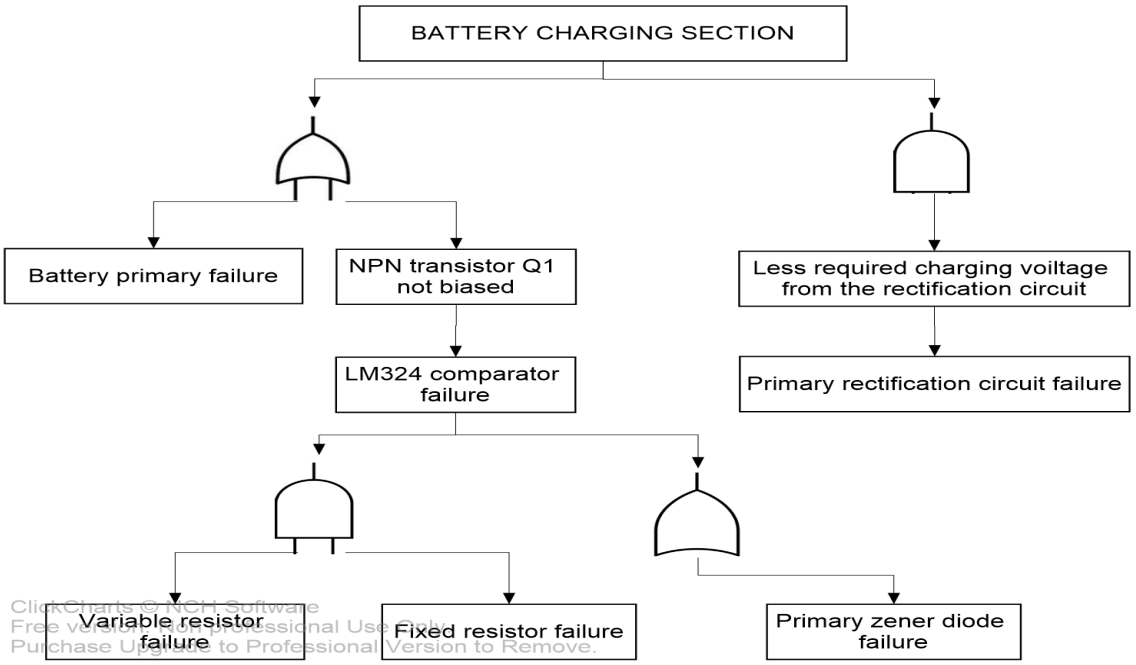

Fig. 3: FTD of the Battery Charging Unit

Fig. 3 presents the Fault Tree Diagram for the battery charging section which was made the top event for the FTD of Fig. 3. The failure rate of the top event was estimated from the primary failure rate of the other components present in the battery charging.

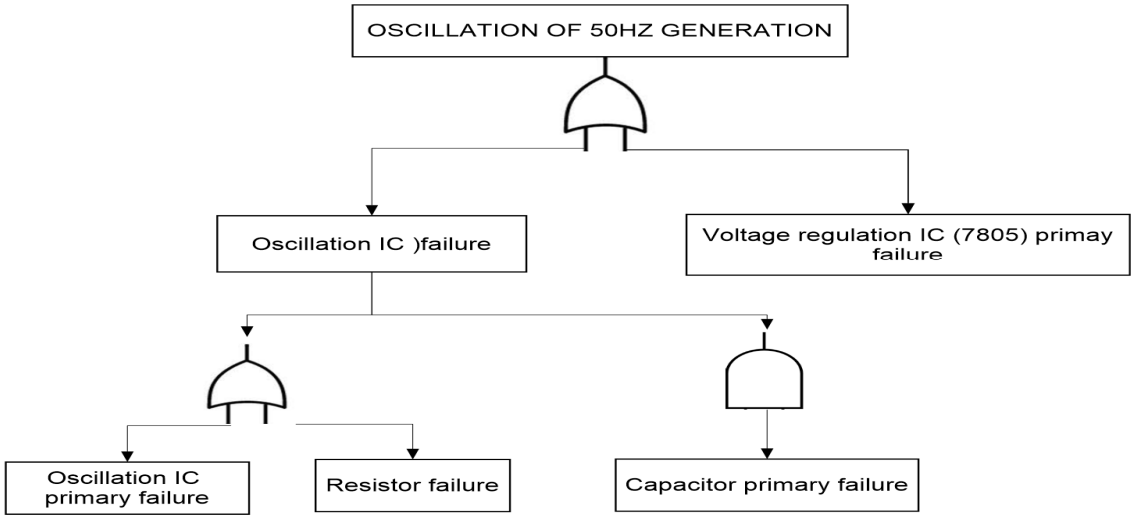

Fig. 4: FTD of the Oscillator Unit

In the oscillation stage, the generation of 50 Hz operating frequency becomes the top event for the FTD of Fig. 4. The failure rate of the top event was estimated from the primary failure rate of the other components present in the oscillation unit.

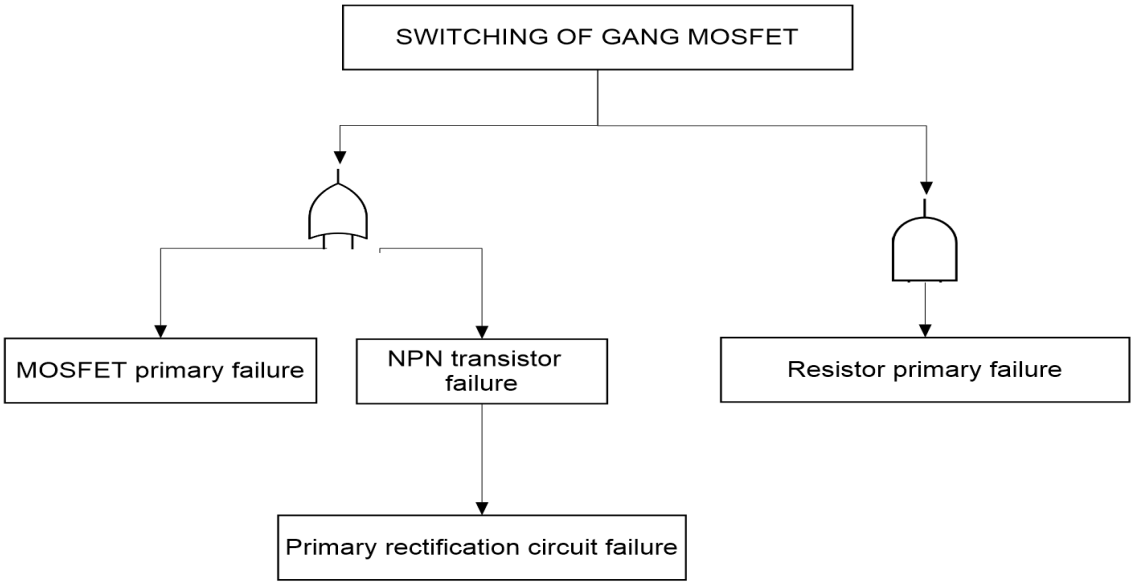

Fig. 5: FTD of the Switching Stage

The switching of the gang MOSFET was made top event for the FTD of Fig. 5. In the Fault Tree Diagram (FTD) of Fig. 5 are two logic gates of OR and AND gates to facilitates the failure rate of the top event which was estimated from the primary failure rate of the other components presented in the circuit of the switching gang MOSFET.

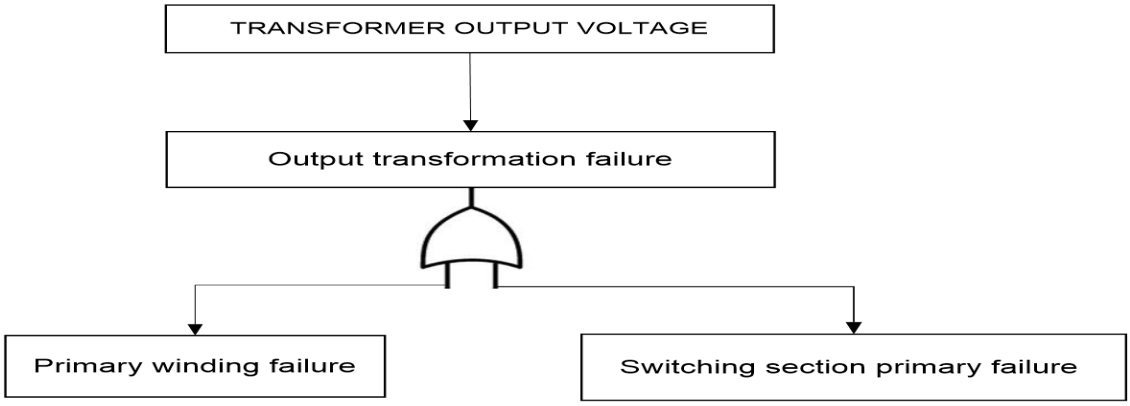

Fig. 6: FTD of the Transformer Output Voltage

The top event of the FTD of Fig. 6 is the output transformer voltage. There is only one OR logic gate that is present in the FTD and the failure rate of the top event was estimated from the primary failure rate of the other components presented along with the output transformer in the circuit diagram.

C. FAILURE RATE ESTIMATION

The standard failure rate values used in the calculation are obtained from the chart of Failure Rate Distribution Table of Military-Standard of - 1629A (MIL-STD-1629A). Also, equations 1 and 2 present the expression for the estimation of failure rate due to an AND and OR gates:

$$\lambda_{AND(1,2)} = f_1 * f_2 \qquad (1)$$

$$\lambda_{OR(1,2)} = (f_1 + f_2) - (f_1 * f_2) \qquad (2)$$

Where f_1 and f_2 are primary failures of system 1 and system 2

Table 2: Failure Rate Values of each Stage

S/N	INVERTER UNIT	FAILURE RATE ESTIMATION
1	**Rectification Stage**	$\lambda_{(A+B)1} = (0.03 + 0.005) - (0.03 * 0.005)$ $= 0.035 - 0.00015$ $= 0.03485$ $\lambda_{(A+B)2} = (0.03485 + 0.0028) - (0.03485 * 0.0028)$ $= 0.03765 - 0.00009758$ $= 0.03755$
2	**Charging Stage**	$\lambda_{(A+B)1} = (0.0085 + 0.0033) - (0.0085 * 0.0033)$ $= 0.00118 - 0.00002805$ $= 0.01177$ $\lambda_{(A*B)1} = 0.01177 * 0.0085$ $= 0.0001000$ $\lambda_{(A*B)2} = 0.0001000 * 0.0028$ $= 0.00000028$ $\lambda_{(A+B)2} = (0.03 + 0.00000028) - (0.03 * 0.00000028)$ $= 0.03000028 - 0.0000000084$ $= 0.030000271$
3	**Oscillator Stage**	$\lambda_{(A*B)} = 0.0085 * 0.00051$ $= 0.00000434$ $\lambda_{(A+B)1} = (0.0035 + 0.00000434) - (0.0035 * 0.00000434)$ $= 0.03504 - 0.00000015$ $= 0.03504$ $\lambda_{(A+B)2} = (0.03504 + 0.0035) - (0.03504 * 0.0035)$ $= 0.03842$
4	**Switching Stage**	$\lambda_{(A+B)2} = (0.014 + 0.0000723) - (0.014 * 0.0000723)$ $= 0.01407 - 0.00000101$ $= 0.01407$

5	**Output Transformation Stage**	$\lambda_{(A+B)1} = (0.03+0.049)-(0.03*0.049)$ $= 0.079 - 0.00147$ $= 0.07753$

Table 2 presents the application of equations 1 and 2 in the estimation of the failure rate values for each of the modularized stages of the 4 kVA inverter systems.

D. ESTIMATION OF THE RELIABILITY VALUES

The reliability of each of the section or stage was estimated using the expression of equation 3:

$$R_{(t)} = 1 - e^{-\lambda t} \qquad (3)$$

where $R_{(t)}$ is the system reliability and it's a function of time t and failure rate λ. Both are the time in second and the system failure rate distribution respectively.

E. RESULTS AND DISCUSSIONS

The failure rate distribution is presented using a bar chart. The bars stand against their respective failure rate estimated values as presented in Fig. 7.

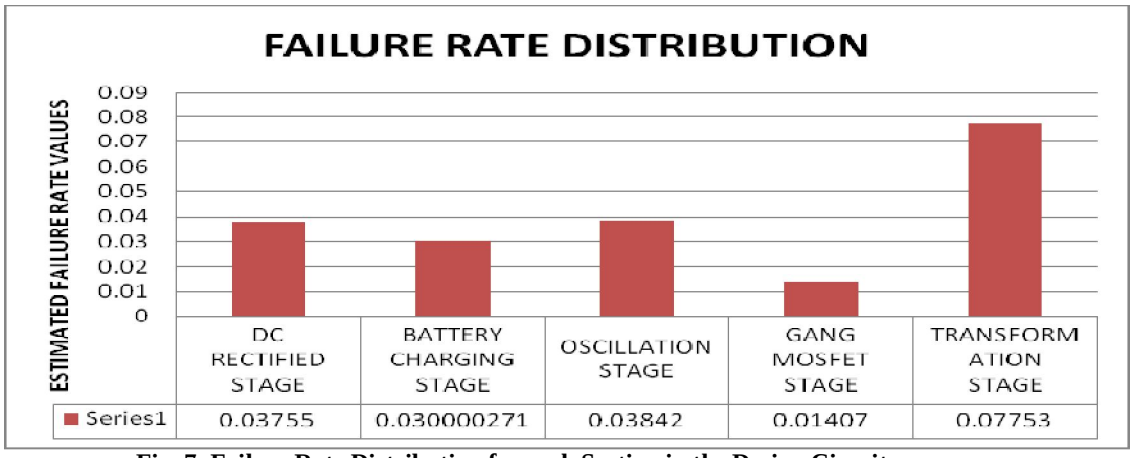

Fig. 7: Failure Rate Distribution for each Section in the Design Circuit

The chart depiction shows that the Gang MOSFET Stage with the lowest failure rate values. These results buttress most manufacturer's claim on MOSFET that, "MOSFET generally shows rigidity while connected and functioning in an electrical circuit than when left unconnected" besides, the Gang MOSFET stage is free of any fragile component, but consist of entire MOSFETs. Also it can be further deduced from the chart that the Output Voltage Transformation Stage depicts the highest failure rate values. This estimated values show that Transformation Stage is very much liable to failure with time.

Fig. 8: DC Rectified Output Stage System's Reliability

Fig. 8 depicts the reliability values of the DC rectified output voltage stage over a time period in hours. It was observed that between 100 hours to 250 hours, the reliability value was below 1 or 100% but there is a fairly rise in the values at 400 hours and beyond.

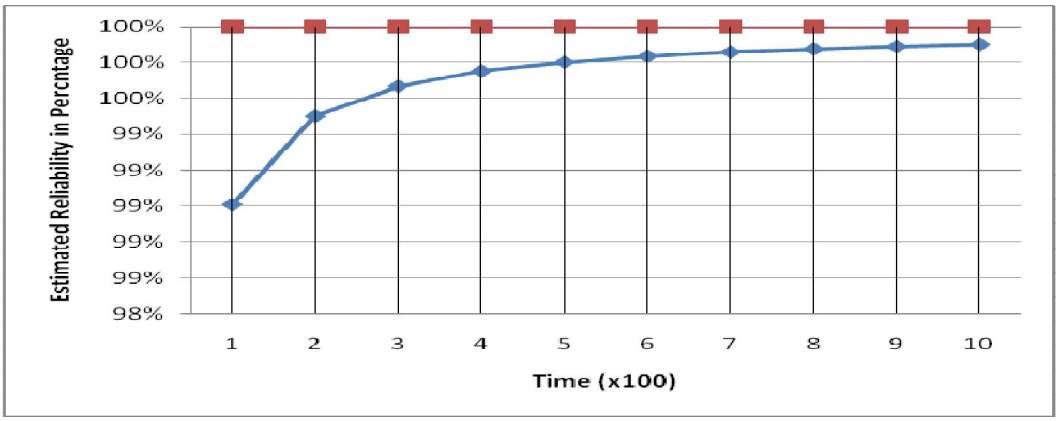

Fig. 9: Battery Charging Stage System's Reliability

Fig. 9 presents reliability depiction of the battery charging stage. Also the reliability values are plotted over time in hours. Approximately the battery charging section reliabilties' values is 1 or 100%.

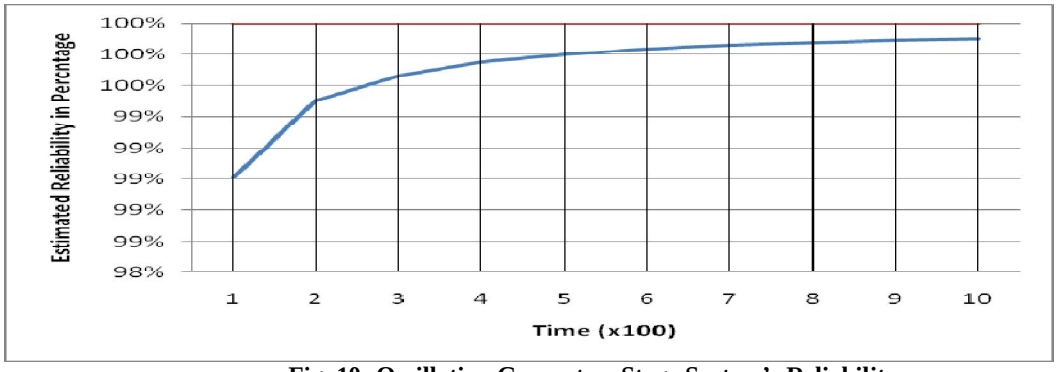

Fig. 10: Oscillation Generator Stage System's Reliability.

The reliabilities' values of the oscillation generator stage is presented in Fig. 10. The time inverter between 100 hours to 200 hours depcits the reliabilities' values to be below 1 and the values appear stable between 500 hours to 600 hours. Hence, there appears no considerable increases in the reliabilities' values.

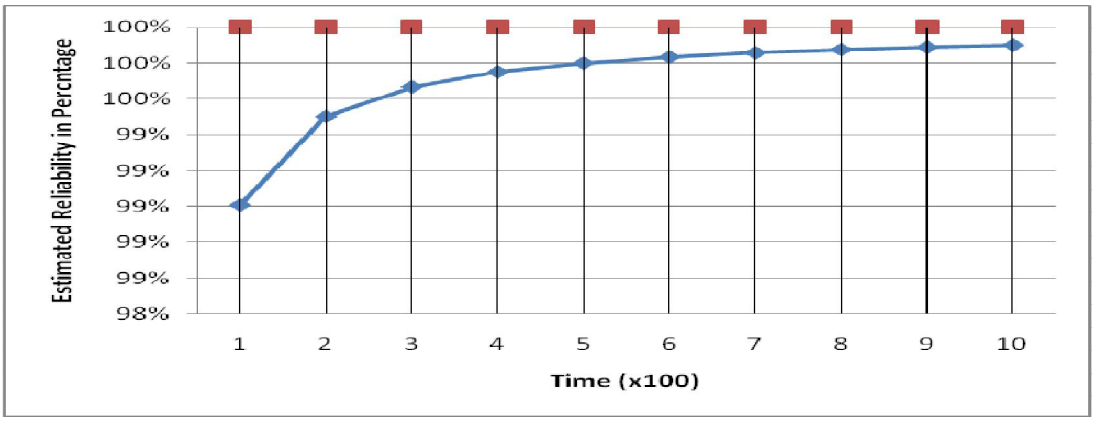

Fig. 11: Gang Mosfet Switching Stage System's Reliability

The depiction of the gang MOSFET swicthing stage reliabilties' values presented in Fig. 11 is not in any shape different from the other reliabilties' values been presented.

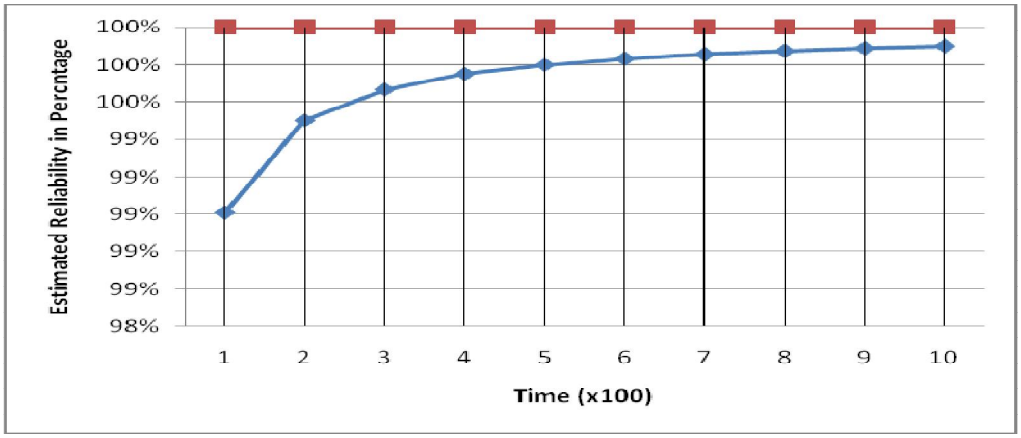

Fig. 12: Voltage Transformation Stage System's Reliability.

Fig. 12 presented the reliabilities' values for the voltage transformation stage. The results show the system reliability to be equal to approximately 1, irrespective of the value of time (t).

Generally from Fig. 8 to Fig. 12, the results indicate that once the system is available (i.e on operation) the reliability remains constant (that is 1.00). In this context the results help to clear the disparity between availability and reliability. Availability is a function of time while Reliability is a function of the circuit components and not of time. Also the types of components, their quantities, their qualities and the manner in which they are arranged within the system have a direct effect on the system's reliability. The relationship between a system and its components is often misunderstood. For example, the following statement is not valid: All of the components in a system have 90% reliability at a given time, thus the reliability of the system is 90% for that time. Unfortunately, poor understanding of the relationship between a system and its constituent components can result in statements like this being accepted as facts, when in reality they are fallacies.

F. THE FAILURE MODES, EFFECTS AND CRITICALITY ANALYSIS (FMECA)

Analysis of potential failure helps design engineers to focus on and understand the impact of potentiatl process or product risk and failures**.** Presented in Table 3 is the investigative development of FMECA worksheet of a modularized 4 kVA inverter systems with an intent to enhance future development of inverter system and identification of specific area of possible improvement.

Table 3: Development of FMECA Worksheet

Circuit Design Specification: 4 KVA, Date Formulated: January 2020, Main Purpose: For Future Development and Specific Area of Improvement.

Failure Modes	Failure Severity (Rated 1 - 10)	Probability of Occurrence	Probability of Detection	Risk Preference Number (RPN)
Rectification Unit	6	0.5	1	3
Charging Unit	4	0.5	1	2
Oscillation Unit	5	0.5	0.5	2.5
Switching Unit	1	0.3	1	0.3
Transformation Unit	9	1	1	9

Presented are five potential failure modes that have been identified. The Risk Preference/Priority Number (RPN) shows that, the Output Voltage Transformation Stage has the highest RPN, followed by the Rectification Stage, Charging Stage, Oscillation Stage and Switching stage with the least RPN. It can be further deduced that, stages with majorly integrated circuit show low RPN while stage with passive components show high RPN and hence should be given more priority or preferences when designing.

IV. CONCLUSIONS

The fault tree diagram and analysis were successfully performed to the study and investigation of the possible potential failure modes. This will help facilitate design alternatives for high reliability at the conceptual design stages.

Also, out of all the five sections as explained, the gang MOSFET stage has the lowest failure rate distribution. This is because the section contains least number component i.e. only MOSFET and resistors connected to its drain terminal. This result depicts that the more the components connected to the section of a system, the higher the tendency of failure in such section and vice-versa. This discovery helps to provide a basis for quantitative reliability, maintainability, safety and logistic analysis during the design stage. This is because the reliability curve results show that once a system is in operation, the reliability of such system remains constant; otherwise the reliability will be zero. Meaning a system will remain reliable in as much it is still in operation and the reliability of any system that is no longer in operation is equal to zero. In this context, the results help to clear the disparity between availability and reliability. Availability is a function of time while reliability is a function of the circuit components and not of time.

On a final note the FMECA table shows that the RPN for the voltage transformation stage is the highest; which indicates that the voltage transformation stage (VTS) should be given the highest priority during the design stage of 4 kVA inverter system and the MOSFET switching unit has the least Risk Preference Number.

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